REMARKS

Claims 1-12 are pending. By this Amendment, new Claims 11-12 are added.

Applicants gratefully acknowledge the indication in the Office Action that Claim 8 contains allowable subject matter.

In the Office Action, the Examiner rejects Claims 1-2 and 7 under 35 U.S.C. § 102(b) over U.S. Patent No. 5,198,746 to Gyugi, *et al.* (Gyugi). The Examiner also rejects Claim 3 under 35 U.S.C. § 103(a) over Gyugyi in view of U.S. Patent No. 6,476,521 to Lof, *et al.* (Lof). The Examiner also rejects Claims 4, 6 and 9-10 under 35 U.S.C. § 103(a) over Gyugyi in view of U.S. Patent No. 3,883,724 to Pradhan, *et al.* (Pradhan). The Examiner also rejects Claim 5 under 35 U.S.C. § 103(a) over Gyugi in view of Lof and Pradhan. These rejections are respectfully traversed.

As noted in further detail after the paragraph summarizing relevant features of Gyugi's disclosure, the Gyugi elements 108, 114, 122, 145, 147, 156 identified by the Examiner as "interfaces" do not disclose or suggest the interfaces recited in Claim 1, because the cited Gyugi elements are "summer-differencing interfaces" or "summer output interfaces" that are *computational elements* for building a sum or difference of two or three input quantities. Furthermore, contrary to the Examiner's assertion, Gyugi at column 8, lines 31-51, does not disclose or suggest computing impedances in the fashion recited in Claim 1. Instead, this passage of Gyugi reducing an inductive line impedance by injecting an AC voltage. Gyugi at column 12, lines 30-39 likewise fails to disclose computing impedance in the fashion recited in Claim 1.

With reference to Gyugi's disclosure, Gyugi is concerned with a series impedance compensation system for a set of power transmission lines (**48a, 48b,**

48c, cf. Fig. 2 and Col. 8, line 19; col. 1, line 8) and the avoidance of disadvantages of conventional capacitive series compensation. It proposes to inject dynamically, i.e., responsive to demand, an AC voltage e_c into a transmission line (**at least into line 48c**; col. 8, line 27). The AC voltage has a distinct phase and amplitude relationship with the transmission line current i_c (Col. 8, lines 28 and 35) and is generated by a solid state switching power converter (reference Numeral 50). An internal control methodology (col. 12, line 40) uses a single current vector describing the three line currents i_a, i_b, i_c instantaneously (col. 12, line 45). The **feedback current vector** with amplitude i_{dqs} and angle Θ is obtained via a vector magnitude calculator 94 and vector phase-locked loop tracker 96, based on the orthogonal components i_{ds} and i_{qs} as derived by transmission line current vector resolver 92. The detailed operation of the three aforementioned means 92, 94, 96 (**corresponding to equations 2 and 3 in Col. 12**) is explained on page 14, line 43, to page 15, line 48, and schematically depicted in Fig. 4. **The single vector current i_{dqs} is then input to a first signal multiplier function 72 (Col. 13, lines 24-27) and can be used to establish a control flow diagram as shown in Fig. 3 (Col. 13, line 19)**.

Returning now to the rejection of Claim 1, the various elements termed "interface" and depicted in Fig. 4 of Gyugyi (reference numerals 108, 114, 122, 145, 147, 156) in fact are "summer-differencing interfaces" (145, Col. 14, line 67; 147, Col. 15, line 11) or "summer output interface" (122, Col. 15, line 45), i.e., they are all *computational elements* for building the sum or difference of two or three input quantities (cf. the signs "+" and "-" next to the corresponding icons in Fig. 4) within the "internal control portion/flow diagram" 100 of the series transformer control 60.

The physical input to the series transformer control 60 occurs via phase sensing of the currents i_a, i_b, i_c from each, phase is sensed with potential or voltage transformers 62a, 62b, 62c (Col. 10, line 37-40). In the context of the present invention, it is the location of these current and voltage transformers, where the local values of the currents and voltages are measured, that constitutes the "interface" between adjacent network sections. Accordingly, only one single interface (per phase) is disclosed by the Gyugyi reference, which can only separate two neighboring sections of a network, but not delimit a transmission section with two ends.

Accordingly, Gyugyi does not show two or more interfaces between a transmission section and other sections of a network (see the interpretation of the term "interface" above). Gyugi likewise fails to disclose or suggest computing impedances - the inductive line impedance XL of the transmission line is not calculated, but reduced by the injected AC voltage e_c, of col. 8, line 25. Accordingly, the passages cited in the Office Action do not appear relevant to an impedance computation.

As Gyugyi is concerned with an improved series impedance compensation system for which obviously one single interface or current/voltage sensing location is sufficient, there is no motivation that would have caused a person of ordinary skill in the art at the time of the invention, to provide a further interface for computing an impedance of the so-defined transmission status of the so-defined transmission section. Accordingly, Gyugi fails to disclose or suggest a method for determining parameters of an equivalent circuit representing a transmission section of an electrical network, where the transmission section is representable as having at least

two interfaces with other sections of the network, wherein the method comprises a) determining, for each of the interfaces a voltage phasor at the interface and a phasor of a current flowing through the interface, the measurements at the different interfaces being made essentially simultaneously, and b) computing, from said voltage and current phasors, values of impedances constituting the equivalent circuit, as recited in Claim 1. Claims 2-12 depend variously from Claim 1, are likewise allowable for at least the same reasons.

With respect to Claims 5 and 11, please note that Pradhan at Column 8, Line 26-40 and in Fig. 3, discloses a Thévenin equivalent voltage of a voltage source in series with a Thévenin impedance connected to a voltage regulated bus. This appears to be the standard notation of Thévenin equivalents, and does not specify how these equivalent values are estimated. In particular, Pradham does not teach or suggest to split the estimation into two stages, comprising the determination of the parameters of the equivalent of the transmission corridor and the computation of a Thévenin equivalent of the feeding generators, nor is Pradhan in any way concerned with a stability analysis of a power network.

Applicants** respectfully submits that the application is in condition for allowance. Favorable consideration on the merits and prompt allowance are respectfully requested. In the event any questions arise regarding this

communication or the application in general, please contact Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

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